CLAIMS

What is claimed is:

1. A method for optimizing at least one numerically controlled delay line (NCDL) in a DDR memory controller, the method comprising:

(a) calculating an offset value for at least one NCDL; and

(b) interpolating a new offset value for the at least one NCDL, based on a change in a delay locked loop (DLL) output value from a previous DLL output value to a new DLL output value.

2. The method of claim 1, wherein the at least one NCDL comprises at least one of a write NCDL, a read NCDL, and a gate NCDL.

3. The method of claim 1, wherein the offset value comprises a final write NCDL offset.

4. The method of claim 1, wherein the offset value comprises a final read NCDL offset.

5. The method of claim 1, wherein the offset value comprises a final gate NCDL offset.

6. The method of claim 1, wherein the interpolating of the new offset value comprises:

interpolating a scaling factor, wherein the scaling factor is a function of the previous DLL output value and the new DLL output value.

7. The method of claim 6, wherein the interpolated new offset value is a function of at least one of the scaling factor and the offset value.

8. The method of claim 1, wherein the previous DLL output value comprises at least one of an original frequency DLL output value and a test frequency DLL output value.

9. The method of claim 8, wherein the interpolating of the new offset value comprises:

interpolating a scaling factor, wherein the scaling factor is a function of the previous DLL output value and the new DLL output value.

10. The method of claim 9, wherein the interpolated new offset value is a function of at least one of the scaling factor and the offset value.

11. The method of claim 1, wherein the interpolating comprises:

deriving an empirical rule, based on at least one of the new DLL output value and a passing window size of a signal;

selecting a step size, based on the empirical rule; and

selecting a new offset value by adjusting a range of values for the at least one NCDL using the selected step size.

12. The method of claim 1, wherein the change in the DLL output value is caused by a change in an operating condition of the DDR memory controller.

13. The method of claim 1, further comprising:

(c) repeating (b) upon a change in an operating condition of the DDR controller.

14. A computer readable media storing a plurality of instructions, wherein execution of the plurality of instructions causes:

(a) calculating an offset value for at least one numerically controlled delay line (NCDL); and

(b) interpolating a new offset value for the at least one NCDL, based on a change in a delay locked loop (DLL) output value from a previous DLL output value to a new DLL output value.

15. The computer readable media of claim 14, wherein the at least one NCDL comprises at least one of a write NCDL, a read NCDL, and a gate NCDL.

16. The computer readable media of claim 14, wherein the offset value comprises a final write NCDL offset.

17. The computer readable media of claim 14, wherein the offset value comprises a final read NCDL offset.

18. The computer readable media of claim 14, wherein the offset value comprises a final gate NCDL offset.

19. The computer readable media of claim 14, wherein the interpolating of the new offset value comprises:

interpolating a scaling factor, wherein the scaling factor is a function of the previous DLL output value and the new DLL output value.

20. The computer readable media of claim 19, wherein the interpolated new offset value is a function of at least one of the scaling factor and the offset value.

21. The computer readable media of claim 14, wherein the previous DLL output value comprises at least one of an original frequency DLL output value and a test frequency DLL output value.

22. The computer readable media of claim 21, wherein the interpolating of the new offset value comprises:

interpolating a scaling factor, wherein the scaling factor is a function of the previous DLL output value and the new DLL output value.

23. The computer readable media of claim 22, wherein the interpolated new offset value is a function of at least one of the scaling factor and the offset value.

24. The computer readable media of claim 14, wherein the interpolating comprises:

deriving an empirical rule, based on at least one of the new DLL output value and a passing window size of a signal;

selecting a step size, based on the empirical rule; and

selecting a new offset value by adjusting a range of values for the at least one NCDL using the selected step size.

25. The computer readable media of claim 14, wherein the change in the DLL output value is caused by a change in an operating condition of the DDR memory controller.

26. The computer readable media of claim 14, further comprising:

(c) repeating (b) upon a change in an operating condition of the DDR controller.